

# REMARKS

Claims 1-19 have been presented for examination in the above-identified U.S. Patent Application.

5

Claims 1-19 have been rejected in Office Action dated March 26, 2004.

Claims 1, 3, 6, 14, 15, and 18 have been amended by  
10 this Amendment A.

Claim 2 has been cancelled by the Amendment A.

Claims 1 and 2-19 are still in the Application and  
15 reconsideration of the application is hereby respectfully requested.

Referring to Paragraph 1 on Page 2 of the Office Action, the drawings have been objected to because of the  
20 lack of designation of Fig. 1 as - -PRIOR ART- -. By this Amendment A, correction to Fig. 1 has been requested implementing the change indicated by Examiner. The proposed change is shown in red on a photocopy of Fig. 1, transmitted herewith. Therefore, objection to the drawings  
25 has been answered by amendment.

Referring to Paragraph 2 and 3 on Page 2 of the OFFICE Action dated March 26, 2004, Claims 6 and 18 have been objected because of informalities kindly pointed out by  
30 Examiner. The informalities pointed out by examiner have corrected by amendment to the Claims. Therefore, objection

to the Claims because of the identified informalities therein has been answered by amendment.

Referring to Paragraphs 4 and 5, Claims 1-4, 6-9, 11-  
5 16 and 18-19 have been provisionally rejected under the  
judicially created doctrine of obviousness-type double  
patenting in view of Claim 4 of co-pending Application No.  
09/920,193. In view of the fact that both of these  
Applications are pending, Applicant believes that it is  
10 premature to address the double patenting rejection at this  
time. Applicant will respond to the double patenting  
rejection when the Claim limitations in both Applications  
are finalized. Applicant thanks the Examiner for bringing  
potential problem to his attention.

15 Referring to Paragraphs 6 and 7 of the Office Action,  
Claim 1-19 have been rejected under 35 U.S.C. 102(b) as  
being anticipated by U.S. Patent 6,096,089 issued in the  
name of Kageshima.

20 Before discussing the Kageshima reference, the  
invention sought to be protected by the present Application  
will be summarized. A detailed simulation model of the  
target processor for power consumption measurements are  
25 desired is generated. Using the simulation model, the  
power consumption for each state of the target processor is  
determined for each state of the target processor. The  
target processor is provided with trace components. The  
trace components are provided in such a manner that the  
30 state of the target processor can be determined. The trace  
signals can be acquired to each clock cycle. The set of  
trace signals from the target processor, applied to the

simulation model, permits the simulation model to recreate the state of target processor in the simulation model. Because the power consumption parameters have been determined for states of the simulation model, the trace-derived simulation model state can be used to determine the power consumption for the target processor. Note that each independent Claims 1, 6, 11, and 18 now make specific reference to the fact that the trace signals themselves are used to determine the state of the simulation model.

Referring next to the Kageshima reference, this reference discloses a simulation model in Col. 1, line 53 through Col. 2, line 7. The reference describes the related art having a gate level simulator. However, the simulation model is executed in the prior art using the object code instructions. Similarly, the invention disclosed by Kageshima adds a trace configuration in the target processor to the related art. However, the trace signals in the Kageshima reference are used to determine the instructions being executed and/or the stall information, cf. Col. 6, lines 51-58. In the invention (first embodiment), the simulation model is run and a directory created relating the power consumption to the instructions. The trace signals are used to develop stall information that can be used to determine an alternative power consumption. Note, in the present information, the trace information is used to establish the state of the target processor, i.e., the status of the gates in the target processor. The technique described by the present Application overcomes the problem that the state of the target machine and the simulation model may differ when the instructions are used as the determinant of the state of

the machine. This result is inherent in the Kageshima reference; otherwise, one would not need a separate power consumption table for the stall state. That is, in the present Application, the state of the target processor is directly transferred to the simulation model. The status of a gate is transferred directly and not inferred from this instruction sequence. In addition, the present invention eliminates the need for two possible power consumption values. In the present invention, because the state of the machine, as determined by the trace signals, is up-dated every clock cycle, there is not need for two power consumption values. The present state of the machine is transferred to the simulation model. (Note that the state determination every clock cycle is included in the Claims.)

Summarizing, the Kageshima reference includes a target processor with trace capability and a gate level simulation model. However, the components are used in a different manner. The Kageshima reference uses the trace signals to determine instruction sequence and stall information, the present invention uses the (expanded) trace information to determine the gate level status of the components and hence the state of the target processor. As implied by the need for two power consumption values, the use of only the instruction information does not specify the state. These differences are not obvious without the teaching of the present invention. Consequently, a rejection under 35 U.S.C. 103 would not be appropriate.

Consequently, in view of the foregoing discussion concerning the Claims now present in Application, it is

believed that Claims 1, 6, 11, and 18 are now in condition for allowance. Therefore, rejection of Claims 1, 6, 11, and 18 under 35 U.S.C. 102(b), or in the alternative under 35 U.S.C. 103, over Kageshima is respectfully traversed.

5

Claims 3-5, 7-10, 12-17, and 19 depend from Claims now believed to be in condition for allowance. Consequently Claims 3-5, 7-10, 12-17 and 19 are believed to be in condition for allowance. Therefore, rejection of Claims 3-  
10 5, 7-10, 12-17, and 19 under 35 U.S.C 102(b), or; in the alternative, under 35 U.S.C. 103 over Kageshima is respectfully traversed.

### CONCLUSIONS

In view of the foregoing discussion and the foregoing  
5 amendments, it is believed that Claims 1 and 2-19 are now  
in condition for allowance of and allowance of Claims 1 and  
2-19 is respectfully requested. Applicant hereby  
respectfully request a timely Notice of Allowance be issued  
in this Application.

10 Should any issues remain that could be resolved by a  
telephonic interview, Examiner is requested to telephone  
the undersigned attorney.

15 Respectfully submitted,



20 William W. Holloway  
Attorney for Applicant  
Reg. No. 26,182

25 Texas Instruments Incorporated  
PO Box 655474, MS 3999  
Dallas, TX 75265  
(281) 274-4064